

Week #	Date	Lecture Topic	Reading	Lab Due	HW Due
1	1 31 Aug (Mon)	Course Introduction	Chap 1		
	2 2 Sep (Wed)	HDL Overview	Chap 2		
	3 3 Sep (Thu)	Lab #1 -- Modelsim Introduction			
2	4 4 Sep (Fri)	Entities, Architectures, and Types	3.1-3.5.1		Chap 1&2
	7 7 Sep (Mon)	Holiday			
	9 9 Sep (Wed)	More Types, Types for Synthesis	3.5-3.7		
3	10 10 Sep (Thu)	Lab #2 --Xilinx Project Navigator		Lab #1	
	11 11 Sep (Fri)	Concurrent Signal Assignment Statements	Chap 4		Chap 3
	14 14 Sep (Mon)	Hierarchical Design	Chap 13		
4	16 16 Sep (Wed)	Processes, Sequential Signal Assignments	5.1-5.4.3		
	17 17 Sep (Thu)	Lab #3 -- 7-Segment Display Controller		Lab #2	
	18 18 Sep (Fri)	If and Case Sequential Statements	5.4.4-5.9		Chap 4, 13, processes
*	21 21 Sep (Mon)	Sequential Circuits (D-FF and RAM)	8.1-8.5.1		
	23 23 Sep (Wed)	Sequential Circuits (Design Examples)	8.5.2, 8.7-8.10		
	24 24 Sep (Thu)	Lab #4 -- VGA Controller		Lab #3	
5	25 25 Sep (Fri)	FSMs and VHDL Descriptions of FSMs	10.1-10.2.1, 10.5-10.5.4		If/Case, Chap 8
	28 28 Sep (Mon)	State encodings, FSM Examples	10.4, 10.6-10.8		
	30 30 Sep (Wed)	Verification Tools in Modelsim	Modelsim Verification Tools		Chap 10
6	1 1 Oct (Thu)	Lab #5 -- UART Transmitter		Lab #4	
	2 2 Oct (Fri)	Midterm #1 (No class)			
	5 5 Oct (Mon)	Testbench Writing	Testbench Notes		
7	7 7 Oct (Wed)	Design for Verification	Design for Verification Notes		
	8 8 Oct (Thu)	Lab #6 -- UART Receiver		Lab #5	
	9 9 Oct (Fri)	Arithmetic -- Fast Adders	Arithmetic Notes		Testbench/Verification
8	12 12 Oct (Mon)	Arithmetic -- Multipliers	Arithmetic Notes		
	14 14 Oct (Wed)	Implementation on FPGAs	FPGA Fabric Notes		
	15 15 Oct (Thu)	Lab #7 -- VGA Terminal Display		Lab #6	
9	16 16 Oct (Fri)	Timing Analysis of Sequential Circuits	8.6, 10.3.2		Addition/Multiplication
	19 19 Oct (Mon)	Parameterized Design Principles	14.1-14.4		
	21 21 Oct (Wed)	Parameterized Design Principles	14.5-14.7		
10	22 22 Oct (Thu)	Lab #8 -- Multipliers		Lab #7	
	23 23 Oct (Fri)	Arithmetic -- CORDIC	CORDIC Notes		Timing, Chap 14
	24 24 Oct (Mon)	Pipelined Design	9.4-9.6		
11	25 25 Oct (Wed)	SRAM Controller	12.3		Pipelining
	29 29 Oct (Thu)	Lab #9 -- Memory Controller		Lab #8	
	30 30 Oct (Fri)	Arithmetic -- Dividers	Arithmetic Notes		
12	27 27 Nov (Mon)	FILE I/O	Notes on FILE I/O		
	4 4 Nov (Wed)	Review / makeup class			CORDIC C Code
	5 5 Nov (Thu)	Lab #10 -- CORDIC, Pipelining, and FILE I/O		Lab #9	
13	6 6 Nov (Fri)	Midterm #2 (No class)			
	9 9 Nov (Mon)	Counters & Poor Sequential Design Practice	9.1-9.2		
	11 11 Nov (Wed)	Registers & RAM	9.3		
14	12 12 Nov (Thu)	Lab #11 -- SRAM Frame Buffer		Lab #10	
	13 13 Nov (Fri)	Clock Skew	16.1-16.2		Chap 9 (not pipelining)
	16 16 Nov (Mon)	Lab day -- question & answer			
15	18 18 Nov (Wed)	Multiple Clock Domains and Metastability	16.3-16.4		
	19 19 Nov (Thu)	Lab #12 -- Etch-a-Sketch		Lab #11	
	20 20 Nov (Fri)	Synchronizer Design & clock domain crossing	16.5-16.6		Skew / Metastability
16	23 23 Nov (Mon)	Handshaking	16.7		
	24 24 Nov (Tue)	Cliff Cummings -- Alumni visit			
	(Fri)	No Class or Lab (Wed-Fri)			
17	30 30 Nov (Mon)	Data transfers across clock domains	16.8		
	2 2 Dec (Wed)	Data Transfer via a memory buffer	16.9-16.12		
	3 3 Dec (Thu)			Lab #12	
18	4 4 Dec (Fri)				Async Data Transfer
	7 7 Dec (Mon)				
	9 9 Dec (Wed)	Review for Final			
	14-18 Dec (M-F)	Final (in the testing center)			
* Last day of lecture for midterm #1					
** Last day of lecture for midterm #2					